

# **Experiment at the LHC Physics Department, Texas A&M University**

# **Upgraded Muon Trigger Development for the CMS** Jeffrey Roe\*, Alexei Safonov, Jason Gilmore, Vadim Khotilovich, Indara Suarez

# **The Standard Model of Particle Physics**

The Standard Model (SM) of particle physics describes the fundamental particles and their interactions. Despite its ability to make predictions which match experimental data with tremendous accuracy, it still has shortcomings. One of these shortcomings is its inability to explain the origin of the masses of the particles it describes. A theoretical solution is the existence of yet another particle, the Higgs boson, which interacts with the other particles of the SM and gives them their mass.

# **The Large Hadron Collider**

The Large Hadron Collider (LHC) is the new highest energy particle accelerator, which collides high energy proton beams to explore the world at the smallest scales ever for new phenomena and interactions.

### **Search for Higgs Boson at LHC**

It is widely expected that the collisions at the LHC will produce the Higgs boson. Discovery of the Higgs boson requires observing its signature decay products in detectors.





LHC Upgrade

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boson or The beam time period. therefore be increased in the next years. This will greatly increase number of r collision seen by the detector

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# **Compact Muon Solenoid (CMS) Experiment and Muon Detection**

CMS is one of two general purpose detectors at the LHC used to perform a broad range of physics measurements and searches for new phenomena.

### **Muon Detection**

Unlike other charged particles, muons are good at penetrating material. Placing the muon sub-detector behind the other detectors (thus providing effective shielding) ensures all we see is muons. Coincidentally, muons also provide one promising search mode for discovery of 

### **Barrel and Endcap Regions**

- The barrel region of the detector uses "drift tubes" (DT) to reconstruct muons
- The endcap region of the detector uses "cathode strip chambers" (CSC)

### **Muon Trigger**

Due to the high collision rate at the LHC (every 25 ns), it is impossible to record every collision event. A "trigger" is therefore implemented in electronics to pick out and record only interesting events. To be effective, this selection process must be extremely fast, requiring state of the art electronics.







# Muon Trigger Upgrade

# Monte Carlo Simulation and Trigger Emulation

Monte Carlo software simulation is used to model the generation of collision events, passage of particles through matter, detector electronics response and trigger logic. This data is used to study the performance of the trigger in different scenarios, e.g.: low and high luminosity, current or upgraded muon trigger, different trigger pt thresholds. 

## **Trigger Efficiency Parameterization**

Probability that the trigger will flag and reconstruct a true muon in an event. For each scenario, efficiency depends on  $\eta$  (muon angle from the beam) and  $p_t$  (muon transverse) momentum). We parameterize and fit each dependence to obtain the final efficiency:

 $\varepsilon_{final}(\eta, p_T) = \varepsilon(\eta; p1, p2, p3) \times \varepsilon(p_T; p4, p5)$ 

A CMSSW function has been written to emulate trigger performance for physics studies with the upgraded detector.

# CMS Upgrade

Without an upgrade, the current trigger must enforce a high p<sub>t</sub> threshold in order to handle the higher particle rates. This severely reduces the efficiency of the detector, most notably in the region where the Higgs boson and other new physics are expected to be. The upgraded detector will be able to handle the higher rates while still enforcing a low p<sub>t</sub> threshold.

0.6

0.4

0.2





- One of the critical updates is the TMB upgrade: • High efficiency requires a more intelligent algorithm to decrease the dead time
- Need a faster, more robust FPGA (Vertex 2  $\rightarrow$  Vertex 6) and therefore a new board design



# **Voltage Regulator Testing: Board Design**

The FPGA going on the new TMB requires 6 stable voltage inputs: 1V (x2), 1.2V, 1.8V, 2.6V, 2.9V. Boards were designed and manufactured in order to test several different voltage regulator options for each supply.

### **Design and Testing Steps**

- 1) Design circuits to meet the required voltage, current, power, etc. specifications using the device datasheet
- 2) Schematic and Printed Circuit Board (PCB) layout using Altium Designer
- 3) Manufacture board in the TAMU Physics Electronics Shop: drill holes, plate with copper, etch tracks
- 4) Solder parts
- 5) Test circuits for voltage stability, operating temperature and radiation tolerance











# **Testing and Analysis**

Test board was powered for extended periods of time (typically multiple 12 hour runs). Regulators were monitored periodically for instabilities in the output voltages (± 10mV).

### **Results**

All tested regulators met stability requirements during continuous operation in the laboratory.

# **Voltage Regulator Testing: Thermal Analysis**

All regulators used on the TMB must operate at a temperature reasonably below their manufacturer specified maximum to ensure a long lifetime for the device.

### Testing

- Thermal images were taken periodically (simultaneous with the voltage stability tests) with a Flir Extech i5 Thermal Imager
- The images were analyzed using the Flir software to determine the external operating temperature of each regulator
- Several "operation modes" were used to simulate possible working conditions in the CMS cavern environment: natural convection, with and without heat sinks, with and without air flow

### Analysis

Temperature measurements were taken on the case of the device, but the manufacturer specified maximum temperatures are given for inside chip. The measured temperature was converted to the internal silicon ("junction") temperature using the thermal resistance given by the Two examples of temperature testing results manufacturer and the power the device is V<sub>CCINT</sub>: 1.0V @ 4A Temperature Results dissipating: 100% of Maxin

# $T_I = T_C + P_D \times R_{\theta IC}$

The ratio of measured temperature to specified maximum temperature was used for comparison

## Results

- All operated below their maximum specified junction temperature
- Some were too close to their maximum to be considered safe for operation at LHC.
- Heat dissipation methods

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# **Voltage Regulator Testing: Stability Analysis**

Electronics system requires that that voltage levels into the FPGA remain stable.

- Plan A: MIC4950 lan B2: MIC6950 Plan C1: LP38853

Plan C2: TPS74901





• Air flow was determined to be the most effective method for removing heat from the regulator circuits (~30% - 40% decrease)

• Thermal heat sinks had a much smaller effect, (~10% decrease), but could be considered as a complementary heat dissipation tool.